DATASHEET

AXP152

Enhanced Power Supply Unit

X-Powers

Catalog

1 . Summary

AXP152 is a highly integrated power management IC that provides easy and flexible power solution for applications that require multi-rail outputs. It has fully met the increasingly complex needs of application processors on accurate power control.

AXP152 integrates an adaptive and USB-compatible PWM charger, four step-down converters (Buck DC-DC converter), seven low dropout regulators. It also features protection circuitry such as over/under-voltage protection (OVP/UVP), over-temperature protection, and over-current protection (OCP) to guarantee the power system security and stability.

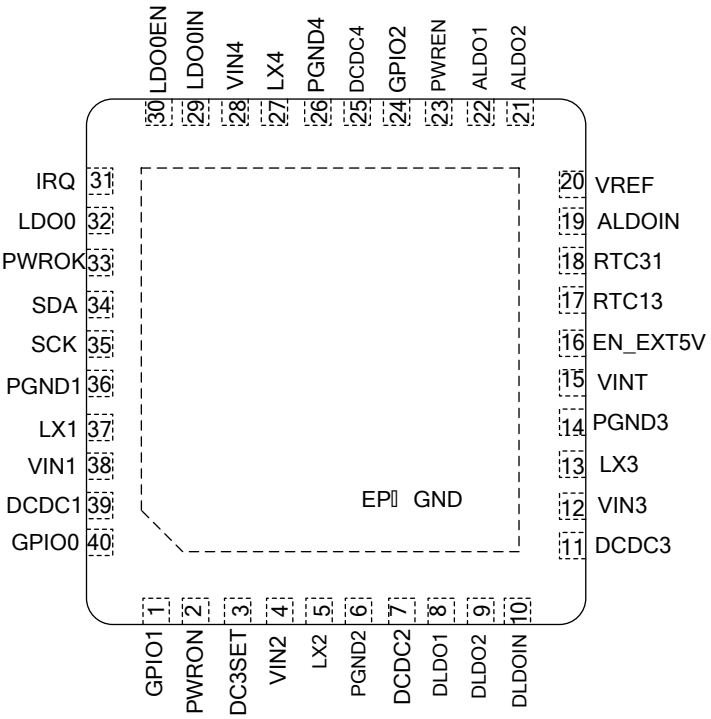
In addition, AXP152 includes a Two Wire Serial Interface (TWSI), through which the application processor is capable of enabling/disabling some power outputs, programming the voltage to decrease the power consumption, and provides customers with unprecedented experience of power management.

AXP152 is available in an 5mm x 5mm 40-pin QFN package。

APPLICATIONS

- Mobile Internet Device,xPad
- Digital Photo Frame, Portable DVD Player, Set-top Box, Entertaining and Education Machine
- Network devices
- Safety monitor
- Application Processor systems

PIN DEFINITION

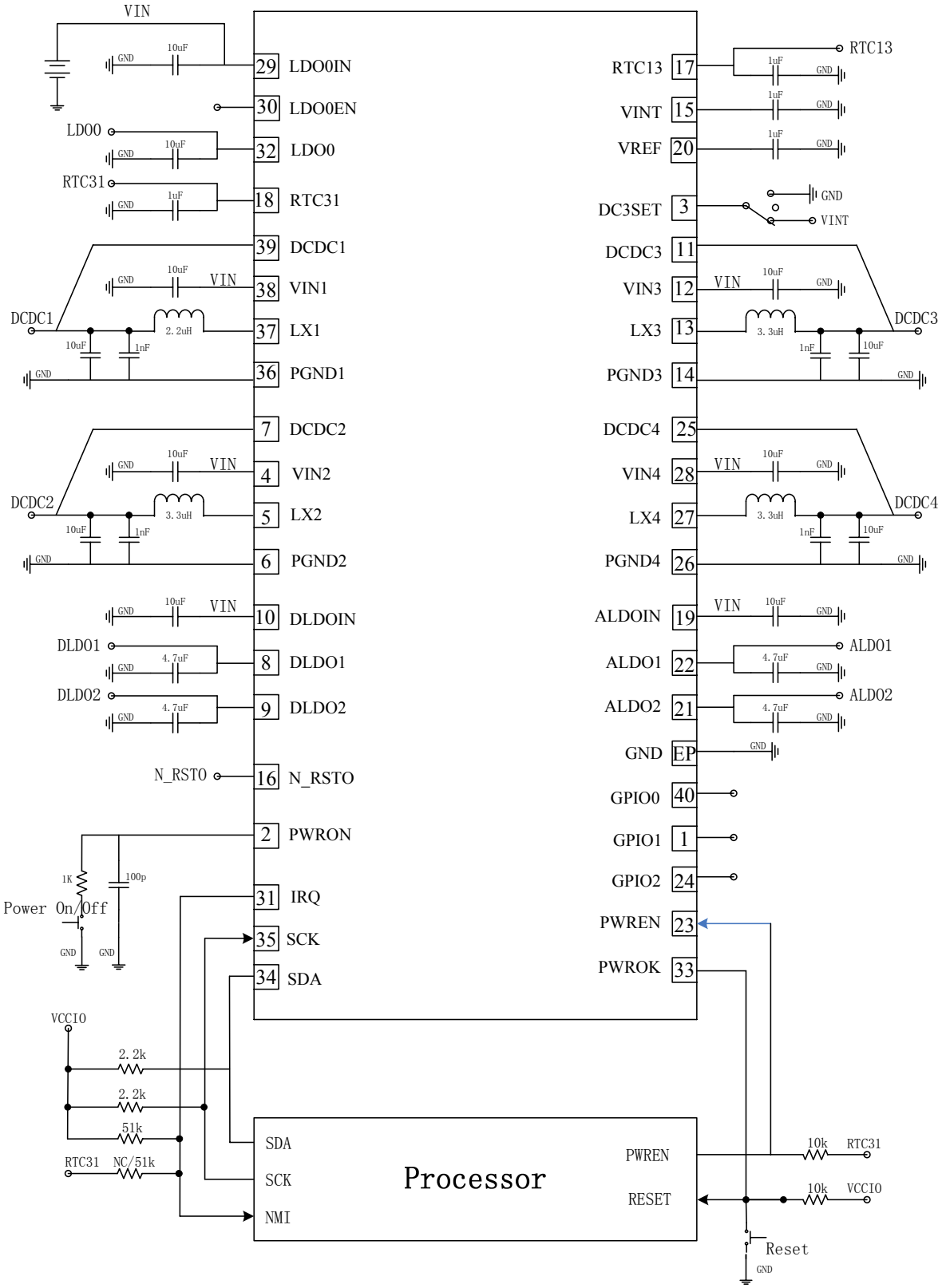


2 . Feature

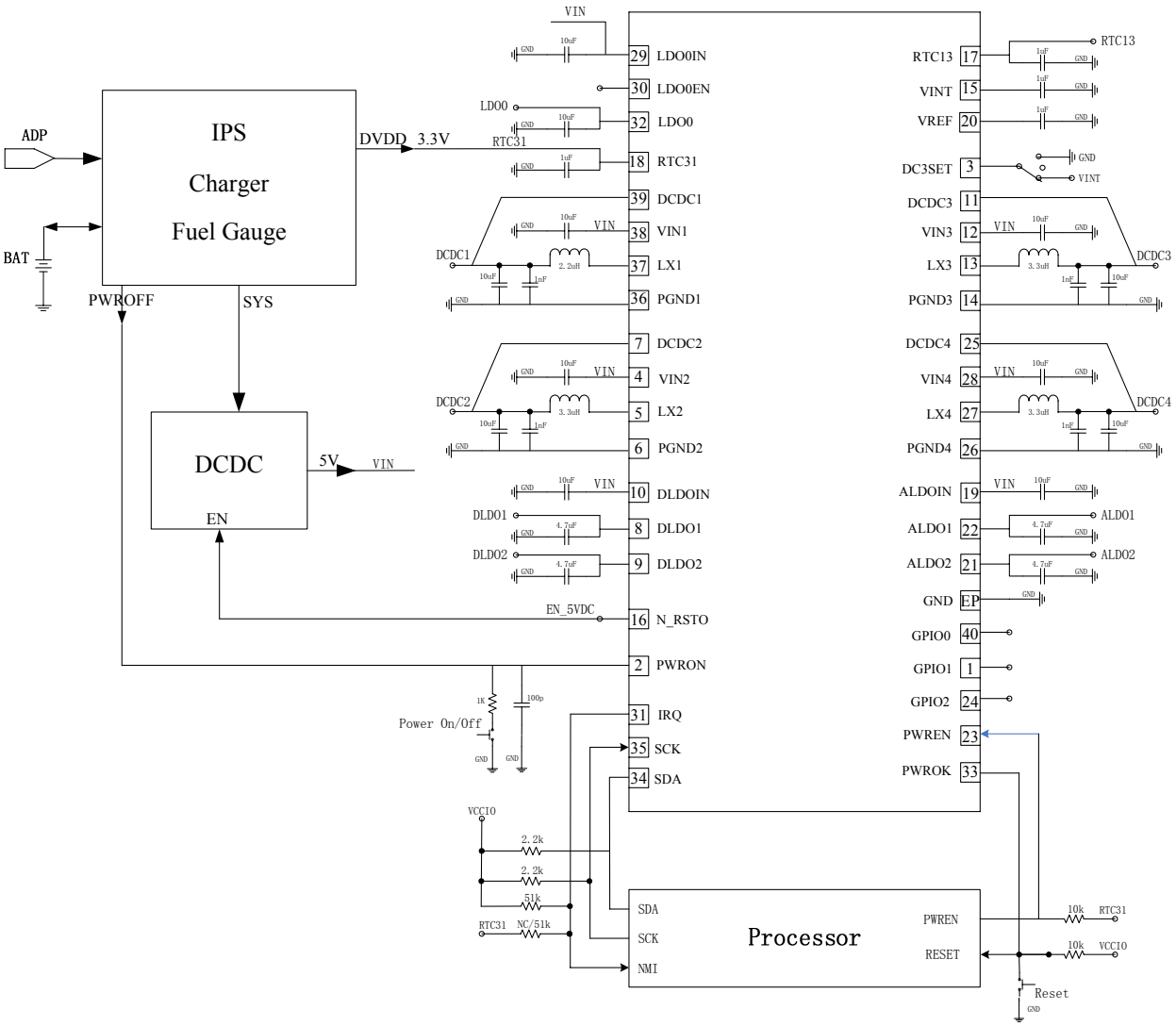
- **4*Buck DC-DC Converters**
  - o DC-DC1：PFM/PWM mode，scaling in 1.7-3.5V,50mV/step，Output current 1A
  - o DC-DC2：PFM/PWM mode,scaling in 0.7-2.275V,25mV/step,Output current 2A, DVM
  - o DC-DC3：PFM/PWM mode，scaling in 1.7-3.5V,50mV/step,Output current 1.2A
  - o DC-DC4：PFM/PWM mode,scaling in 1.7-3.5V,25mV/step,Output current 1.2A
- **System Management**
  - o Support software shutdown or hardware power off
  - o External wakeup source
  - o Output monitor
  - o PWROK signal for reset or power off
  - o OVP/UVP
  - o Programable power on voltage or sequence
- **7 LDOs**
  - o LDO0：Output current 1.5A,Internal 500/900/1500mA current limited option
  - o RTCLDO：on for RTC31，output 3.1V, One for RTC13,Output 1.3/1.8V
  - o ALDO1：Analog LDO，scaling in 1.2-3.3V, 300mA
  - o ALDO2：Analog LDO，scaling in 1.2-3.3V, 300mA
  - o DLDO1：Digtal LDO or Switch，scaling in 0.7-3.5V,100mV/step,300mA
  - o DLDO2：Digtal LDO or Switch，scaling in 0.7-3.5V,100mV/step,300mA
  - o GPIOLDO：low noise LDO, scaling in 0.7-3.5V,100mV/step,30mA
- **Host Interface**
  - o Programable Interrupt and wakeup management
  - o Multi-function Pins
  - o Internal Timer

3．Typical Application

- **For single-cell or no battery applications**



- **For multi-cell battery applications**



4．Absolute Maximum Ratings

Symbol	Description	Value	Units
LDO0IN	Input Voltage	-0.3 to 11	V
ALDOIN	Input Voltage	-0.3 to 6	V
T_J	Operating Temperature Range	-40 to 130	℃
Ts	Storage Temperature Range	-40 to 150	℃
T_{LEAD}	Maximum Soldering Temperature (at leads，10sec)	300	℃
V_{ESD}	Maximum ESD stress voltage，Human Body Model	>4000	V
P_D	Internal Power Dissipation	2000	mW

5．Electrical Characteristics

V_{LDO0IN} =5V， V_{ALDOIN} =3.8V， T_A= 25℃

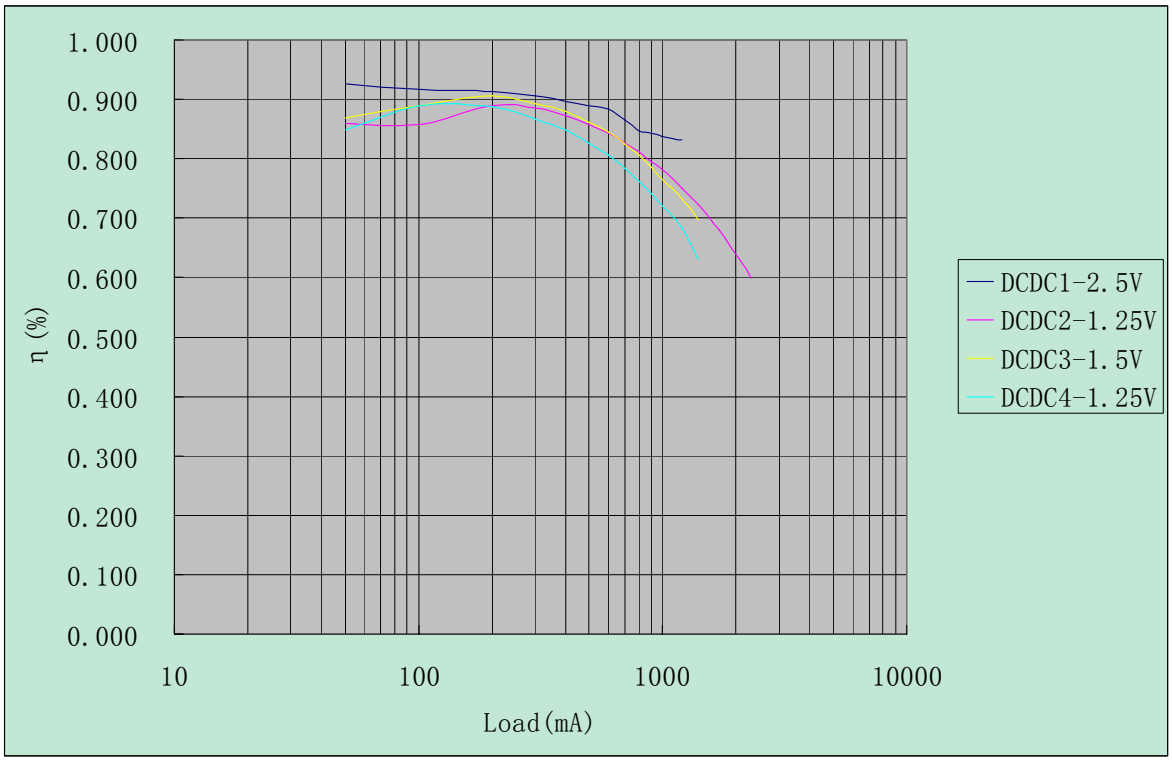
SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
LDO0IN						
V_{IN}	LDO0IN Input Voltage		3		6.8	V
ALDOIN						
V_{IN}	ALDOIN Input Voltage		3		5.5	V
V_{UVLO}	ALDOIN Under Voltage Lockout	Default		3.3		V
Off Mode Current						
I_{OFF}	OFF Mode Current	LDO0IN=ALDOIN= 0V, RTC31=3.3V		15		μA
Logic						
V_{IL}	Logic Low Input Voltage			0.3		V
V_{IH}	Logic High Input Voltage			2		V
TWSI						
V_{CC}	Input Supply Voltage			3.3		V
ADDRESS	TWSI Address	Default		0x60		
f_{SCK}	Clock Operating Frequency			400		kHZ
t_f	Clock Data Fall Time	2.2Kohm Pull High		60		ns
t_r	Clock Data Rise Time	2.2Kohm Pull High		100		ns
DCDC						
f_{OSC}	Oscillator Frequency	Default		2.25		MHz
SYMBOL	**DESCRIPTION**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
DCDC1						
I_{VIN1}	Input Current	PFM Mode		45		μA

		I_{DC1OUT} =0				
I_{LIM1}	PMOS Switch Current Limit	PWM Mode		1600		mA
I_{DC1OUT}	Available Output Current	PWM Mode		1000		mA
V_{DC1OUT}	Output Voltage		1.7	3.3	3.5	V
DCDC2						
I_{VIN2}	Input Current	PFM Mode I_{DC2OUT} =0		20		μA
I_{LIM2}	PMOS Switch Current Limit	PWM Mode		2400		mA
I_{DC2OUT}	Available Output Current	PWM Mode		2000		mA
V_{DC2OUT}	Output Voltage Range		0.7	1.25	2.275	V
DCDC3						
I_{VIN3}	Input Current	PFM Mode I_{DC3OUT} =0		45		uA
I_{LIM3}	PMOS Switch Current Limit	PWM Mode		1600		mA
I_{DC3OUT}	Available Output Current	PWM Mode		1200		mA
V_{DC3OUT}	Output Voltage Range		0.7	2.5	3.5	V
DCDC4						
I_{VIN4}	Input Current	PFM Mode I_{DC3OUT} =0		45		uA
I_{LIM4}	PMOS Switch Current Limit	PWM Mode		1600		mA
I_{DC3OUT}	Available Output Current	PWM Mode		1200		mA
V_{DC3OUT}	Output Voltage Range		0.7	1.25	3.5	V
LDO0						
V_{LDO0}	Output Voltage	I_{LDO1}=1mA	-1%	5 3.3 2.8 2.5	1%	V
I_{Limit}	Output Current Limited			Not 1500 900 500		mA
I_Q	Quiescent Current			55		μA
R_{DSON}	V_{LDO0}=5V, I_{LDO0} not limited	PIN to PIN,LDO0IN to LDO0		200		mΩ
RTC31						
V_{RTC31}	Output Voltage	I_{RTC31}=1mA	-1%	3.1	1%	V
I_{RTC31}	Output Current			30		mA
SYMBOL	**DESCRIPTION**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
RTC13						
V_{RTC13}	Output Voltage	I_{RTC31}=1mA	-1%	1.3	1%	V

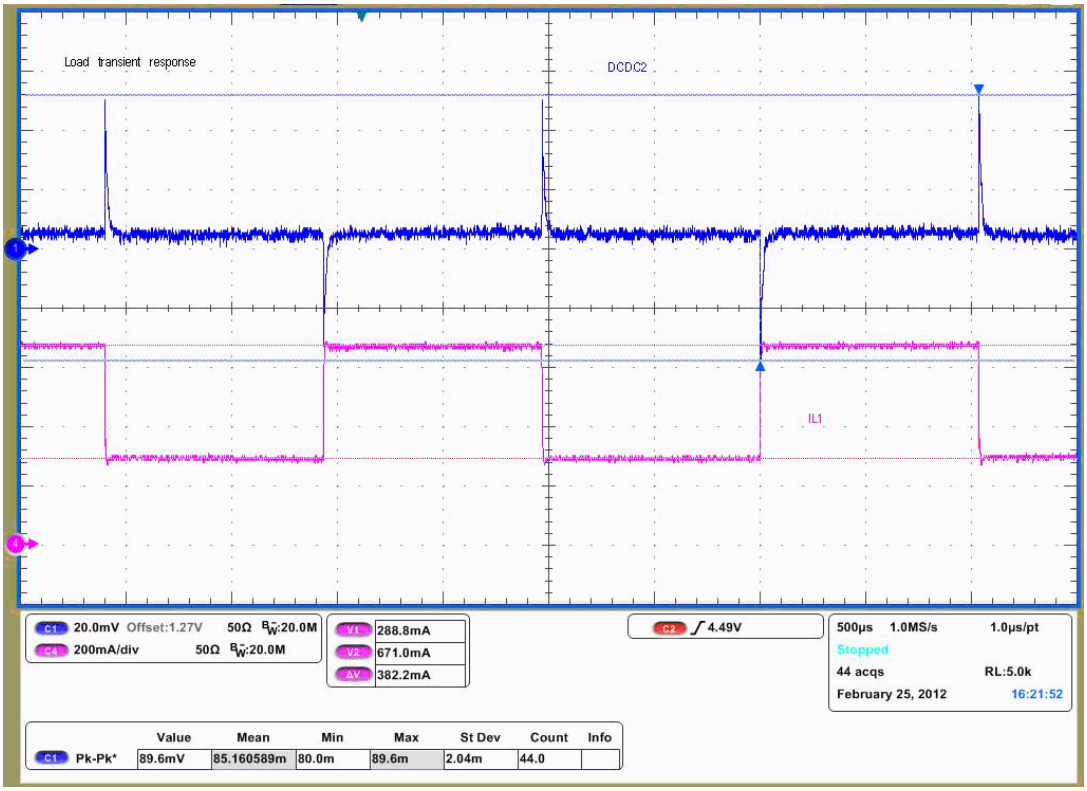
				1.8		
I_{RTC13}	Output Current			30		mA
ALDO1						
V_{ALDO1}	Output Voltage	I_{ALDO1}=1mA	-1%	3	1%	V
I_{ALDO1}	Output Current			300		mA
I_Q	Quiescent Current			55		μA
PSRR	Power Supply Rejection Ratio	V_{ALDOIN} =4.2V,Vo=1.8V, I_{ALDO1}=10mA，1KHz		85		dB
e_N	Output Noise,<20KHz	V_{ALDOIN} =3.6V,Vo=1.8V , Io=60mA		43		μV_{RMS}
ALDO2						
V_{ALDO2}	Output Voltage	I_{ALDO2}=1mA	-1%	1.2	1%	V
I_{ALDO2}	Output Current			300		mA
I_Q	Quiescent Current			55		μA
PSRR	Power Supply Rejection Ratio	V_{ALDOIN} =4.2V,Vo=1.8V, I_{ALDO2}=10mA，1KHz		81		dB
e_N	Output Noise,<20KHz	V_{ALDOIN} =3.6V,Vo=1.8V , Io=60mA		38		μV_{RMS}
DLDO1						
V_{DLDO1}	Output Voltage	I_{DLDO1}=1mA	-1%	2.8	1%	V
I_{DLDO1}	Output Current			300		mA
I_Q	Quiescent Current			55		μA
PSRR	Power Supply Rejection Ratio	V_{DLDOIN} =4.2V,Vo=1.8V, I_{DLDO1}=10mA，1KHz		55		dB
DLDO2						
V_{DLDO2}	Output Voltage	I_{DLDO2}=1mA	-1%	1.8	1%	V
I_{DLDO2}	Output Current			300		mA
I_Q	Quiescent Current			55		μA
PSRR	Power Supply Rejection Ratio	V_{DLDOIN} =4.2V,Vo=1.8V, I_{DLDO2}=10mA，1KHz		55		dB
GPIOLDO						
$V_{GPIOLDO}$	Output Voltage	$I_{GPIOLDO}$=1mA	-1%	2.8	1%	V
$I_{GPIOLDO}$	Output Current			20		mA
I_Q	Quiescent Current			123		μA
e_N	Output Noise,<20KHz	V_{ALDOIN} =3.6V,Vo=1.8V , Io=60mA		37		μV_{RMS}

6．Typical Characteristics

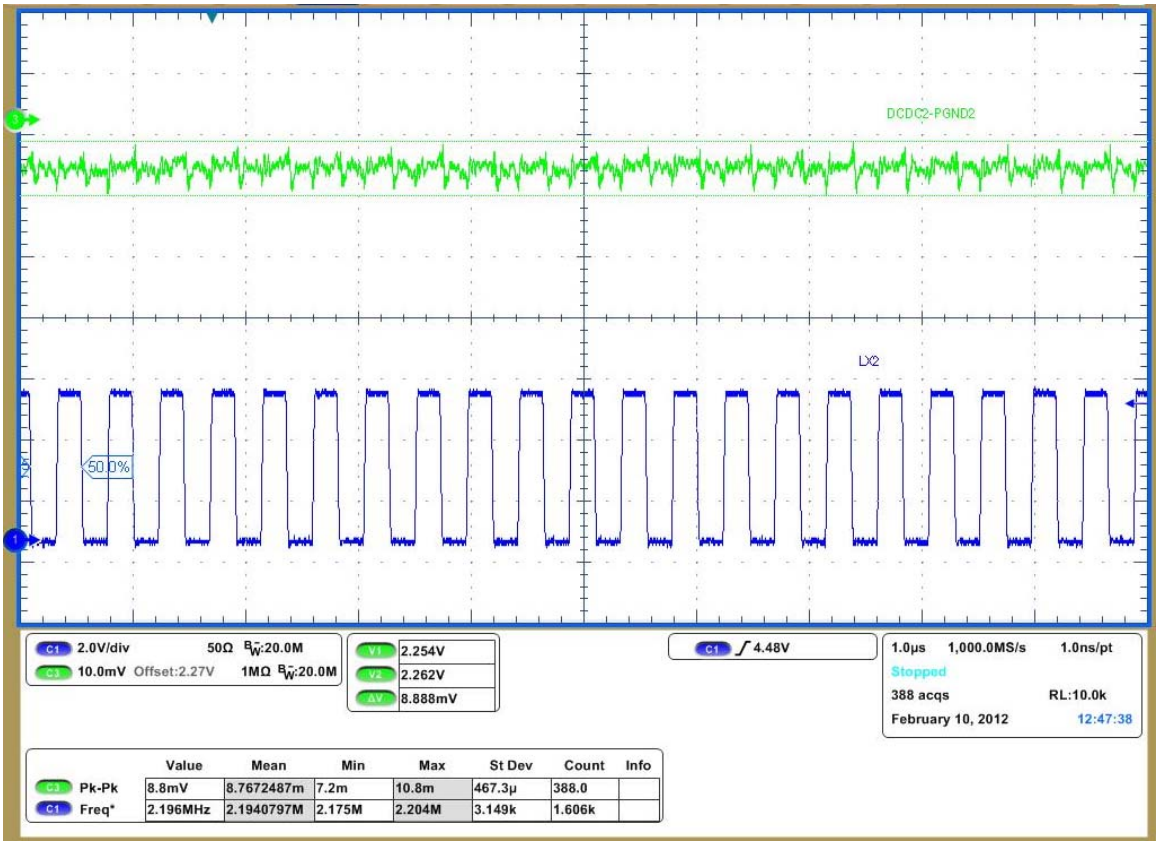
DCDC Efficiency vs. Load(3.8Vin)



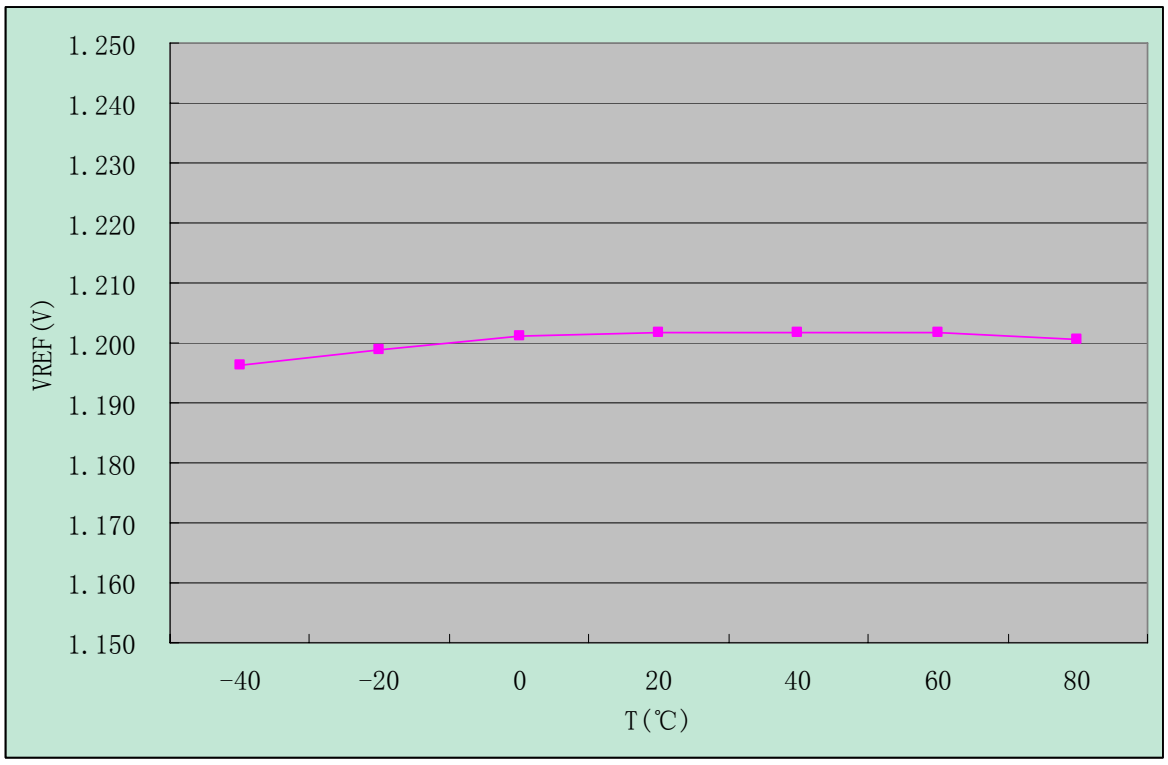
DC-DC Load Transient(Typical:DCDC2 0.3~0.7A)



DC-DC Ripple



V_{REF} vs Temperature

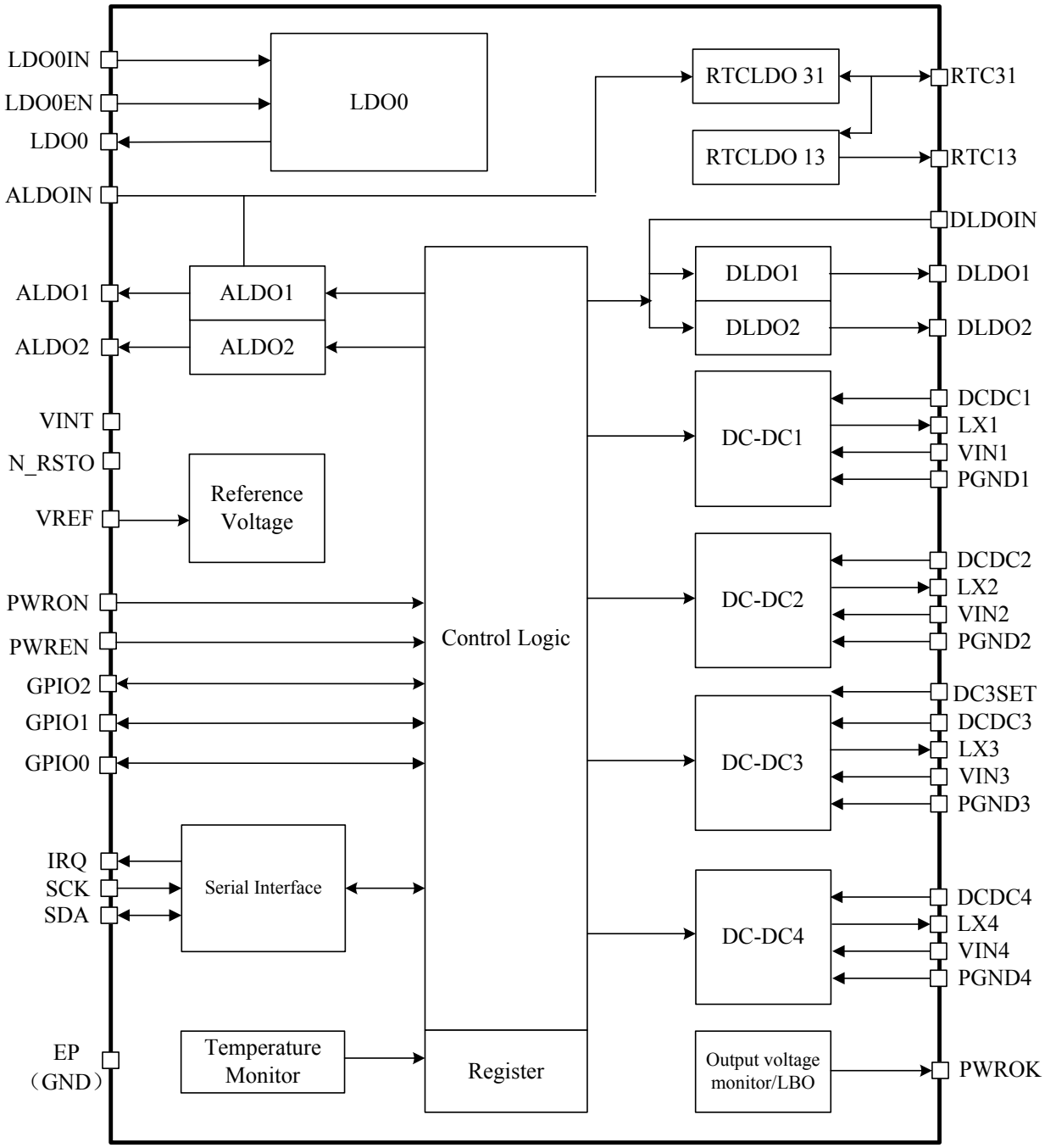


7．Pin Description

Num	Name	Type	Condition	Function Description
1	GPIO1	IO	REG91[2:0]	GPIO1
2	PWRON	I		Power On-Off key input，Internal 100k pull high to APS
3	DC3SET	I		Set the default output voltage for DCDC3
4	VIN2	PI		DCDC2 input source
5	LX2	IO		Inductor Pin for DCDC2
6	PGND2	G		NMOS Ground for DCDC2
7	DCDC2	I		DCDC2 feedback pin
8	DLDO1	O		Output Pin of DLDO1
9	DLDO2	O		Output Pin of DLDO2
10	DLDOIN	PI		DLDO1/2 input source
11	DCDC3	I		DCDC3 feedback pin
12	VIN3	PI		DCDC3 input source
13	LX3	IO		Inductor Pin for DCDC3
14	PGND3	G		NMOS Ground for DCDC3
15	VINT	PO		Internal logic power, 2.5V
16	EN_EXT5V	O		Output enable signal for external power module
17	RTC13	O		RTC power output for HOST RTC block
18	RTC31	IO		RTC power output or input for HOST RTC block
19	ALDOIN	PI		Power supply for analog and ALDO1/2
20	VREF	O		Internal reference voltage
21	ALDO2	PO		Output Pin of ALDO2
22	ALDO1	PO		Output Pin of ALDO1
23	PWREN	IO		Enable input for some power module ,could be configed for GPIO3(REG93[3:0])
24	GPIO2	IO	REG92[2:0]	GPIO2
25	DCDC4	I		DCDC4 feedback pin
26	PGND4	G		DCDC4 input source
27	LX4	IO		Inductor Pin for DCDC4
28	VIN4	PI		NMOS Ground for DCDC4
29	LDO0IN	PI		LDO0 input source
30	LDO0EN	I		Enable input for LDO0
31	IRQ	IO		IRQ output
32	LDO0	PO		Output Pin of LDO0
33	PWROK	O		Power Good Indication OutPut
34	SDA	IO		Data pin for serial interface,normally it connect a 2.2K resistor to 3.3V I/O power
35	SCK	I		it is the Clock pin for serial interface,normally it connect a

				2.2K resistor to 3.3V I/O power
36	PGND1	G		NMOS Ground for DCDC1
37	LX1	IO		Inductor Pin for DCDC1
38	VIN1	PI		DCDC1 input source
39	DCDC1	I		DCDC1 feedback pin
40	GPIO0	IO	REG90[2:0]	GPIO0
41	EP(GND)	G		Exposed Pad, need to connect to system ground

8．Functional Block Diagram



9 . Control and Operating

When AXP152 works, SCK/SDA pin of TWSI interface are pulled up to the system IO power, so Host can conduct flexible monitoring and adjustment for AXP152 operation via this interface(SIEN=1).

If you not need TWSI,then connect SCK to ALDOIN,the AXP152 work in Stand-Alone mode(SIEN=0).

NOTE:

✧ The " host " refers to the main processor of application system.

9.1 Power On/Off & Reset

Power Enable Key (PEK)

The Power Enable/ Sleep/Wakeup Key can be connected between PWRON pin and GND of AXP1522. AXP152 can automatically identify the “Long-press” and “Short-press” and then correspond respectively.

Power on Source

1. ALDOIN insert
2. PEK longer than “ONLEVEL”
3. When SIEN=1 and Reg8F[7]=1, an longer than 16ms negative pulse on IRQ pin

Power On

After power on, DC-DC and LDO will be soft booted in preset timing sequence, and then either Host or PWREN pin can enable/disable corresponding power.

Power Off

When you push-and-hold PEK longer than IRQLEVEL, HOST can write “1” into“REG32H [7]” to inform AXP152 to shutdown, which can disable all power output except RTCLDO.

System power-off is initiated whenever the following conditions occur:

1. Input voltage is too low(Low-Power Protection)
2. Power output voltage is too low due to overload(Overload Protection)
3. Input voltage is too high(Overvoltage Protection)
4. Push PEK longer more than OFFLEVEL(Default 6S), and system will cut off all power output except RTCLDO(there is no need for an extra RESET key)

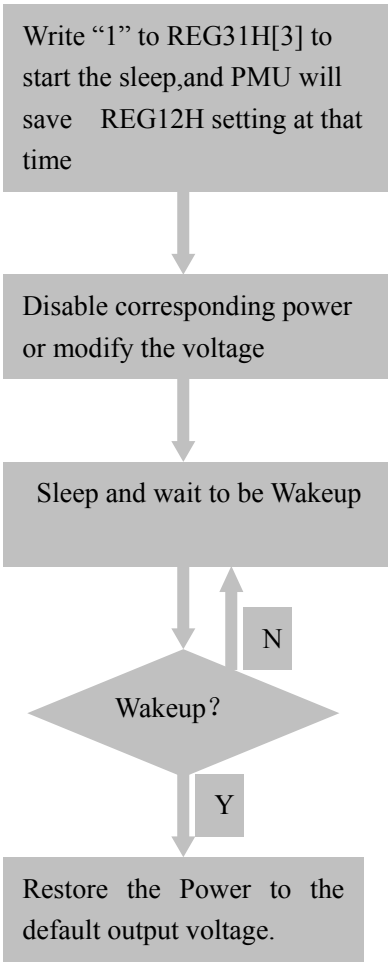
Remarks: With the automatic protection mechanism, AXP152 can protect whole system by preventing Components from irriversable damage due to system abnormality.

Sleep and wakeup

When the running system needs to enter Sleep mode, REG31H [3] will determine whether one or several power rails should be disabled or change to other voltage. Wakeup can be triggled by either LDO0IN low go high,PEK signal, or the rising/falling edge of GPIO0、GPIO1、GPIO2、GPIO3 (To be the rising or falling edge, or both can be programmed by REG90H[7:6]、REG92H[7:6]、REG93H[7:6] and REG95H[7:6]), with all power rails resume to default voltage in default power on timing sequence.

NOTE: PEK IRQ（REG42H[1]）、GPIO0 INPUT Edge IRQ（REG44H[0]）、GPIO1 INPUT Edge IRQ（REG44H[1]）、GPIO2 INPUT Edge IRQ（REG44H[2]）、GPIO3 INPUT Edge IR（REG44H[3]）should be “Enable” to notify the processor to exit Sleep Mode via IRQ PIN.

See control process under sleep and wakeup modes as below:



System Reset and Output Monitoring (PWROK)

The PWROK in AXP152 can be used as the reset signal of application system. During AXP152 startup,

PWROK outputs low level, which will then be pulled high to startup and reset the system after each output voltage reaches the regulated value.

When application system works normally, AXP152 will be always monitoring the voltage and load status. If overload or under-voltage occurs, the PWROK will instantly drive low to reset the system and prevent data losses.

9.2 Multi-Power Outputs

The following table has listed the multi-power outputs and their functions of AXP152:

Outputs	Type	Default	Application	Current
DCDC1	BUCK	Configurable	3.3V I/O	1000 mA
DCDC2	BUCK	Configurable	1.25Vcore	2000 mA
DCDC3	BUCK	Configurable	1.5Vddr	1200 mA
DCDC4	BUCK	Configurable	1.25Vcpu	1200 mA
RTCLDO	LDO	3.1/1.3/1.8V	RTC	30 mA
LDO0	LDO	Configurable		
ALDO1	LDO	Configurable		300 mA
ALDO2	LDO	Configurable		300 mA
DLDO1	LDO	Configurable		300 mA
DLDO2	LDO	Configurable		300 mA
GPIOLDO	LDO	Configurable		20 mA

AXP152 includes four synchronous step-down DC-DCs, seven LDOs, as well as multiple timing and controlling methods. The work frequency of DC-DC is 2.25MHz by default, which is adjustable via registers. External small inductors and capacitors can be connected as well. In addition, all DC-DCs can be set in PWM mode or auto mode (automatically switchable according to the load). See register REG80H.

DC-DC1/2/3/4

DCDC1 output voltage ranges from 1.7-3.5V，DCDC2 output voltage ranges from 0.7-2.275V，DCDC3/4 output voltage ranges from 0.7-3.5V (refer to “REG23H 26H 27H 2BH”)。

output capacitor is recommended to use low ESR ceramic capacitors above 10uF X7R；when the output voltage is set above 2.5V，2.2uH inductors is recommended; when the output voltage is set under 2.5V，3.3uH inductors is recommended. Besides, the inductor saturation current should be larger than 50% of the largest demanded current in power circuitry.

Inductor Recommendation List:

Inductors		
Module NO.	**Current Spec**	**DC Internal Resistance**

Murata LQH55PN2R2NR0	2100mA@2.2uH	30mOhm
Murata LQH55PN4R7NR0	1400mA@4.7uH	60mOhm
Murata LQH44PN2R2MP0	2000mA@2.2uH	49mOhm
Murata LQH44PN4R7MP0	1700mA@2.2uH	80mOhm
TDK VLF5010ST-2R2M2R3	2700mA@2.2uH	41mOhm
TDK VLF5014ST-4R7M1R7	1700mA@4.7uH	98mOhm
TDK SLF6045T-4R7N2R4-3PF	2400mA@4.7uH	27mOhm
Capacitors		
Module NO.	**Temperature spec**	**Allowance**
TDK C2012X5R0J475K	X5R/X7R	10%@4.7uF
TDK C2012X5R0J106K	X5R/X7R	10%@10uF
Murata GRM31E71A475K	X7R	10%@4.7uF
Murata GRM21E71A106K	X7R	10%@10uF
Murata GRM31E71A106K	X7R	10%@10uF

RTCLDO

RTCLDO31/13 are always on and can be used to supply continuous power for application RTC with 30mA drive ability,it can be set to 3.1V/1.3V/1.8V.

LDO0

LDO0 can be set to LDO or current switch,LDO0EN is the enable signal of LDO0;If LDO0EN=Low,LDO0 can be enabled by REG15H[7]. If it set to be current switch,the current can be set to 500/900/1500mA through REG15H[0:1].

ALDO1/2

ALDO1/2 low noise LDO，and can be used to supply power for analog circuits of application system.

DLDO1/2

DLDO1/2 can supply power for systems like SRAM or PLL with 300mA drive ability.

GPIOLDO

GPIOLDO also as a low noise LDO, and its drive ability is 20mA.

Soft Start

All DC-DCs and LDOs support soft start which can avoid the impact of dramatic current change on

the input path in system boot stage.

Self-Diagnosis: Load Monitoring and Current-Limit Protection

All DC-DCs and LDOs support load monitoring and current-limit functions. When the load current exceeds its drive ability, all output voltage will decrease to protect the internal circuits. When the DC-DCs output voltage is lower than 85% of the set voltage, AXP152 will automatically shutdown.

All DC-DCs do not require external Schottky diodes and resister divider feedback circuits. If a certain DC-DC is unnecessary in application, just float the corresponding LX pins.

9.3 Default Voltage/Timing Setting

The default voltage and power on sequence of each power can be set by AXP152.

power on sequence includes eight levels, and the interval between each level can be set as 1、4、16 and 32mS.

Default voltage setting: each DC-DC/LDO setting ranges from the lowest voltage to the highest voltage.

Internal set	DC3SET=VINT	DC3SET=GND	DC3SET floating
0	1.8V	1.5V	1.2V
1	3.3V	2.8V	2.5V

9.4 Multi-Function Pin Description

GPIO[3:0]

Can be defined as GPIO[3:0], Please refer to REG90H-96H Instruction for details

PWREN

Default as PWREN,control power rails as preset,and it can be set to GPIO3,pull-up it to RTC31 as recommended.

EN_EXT5V

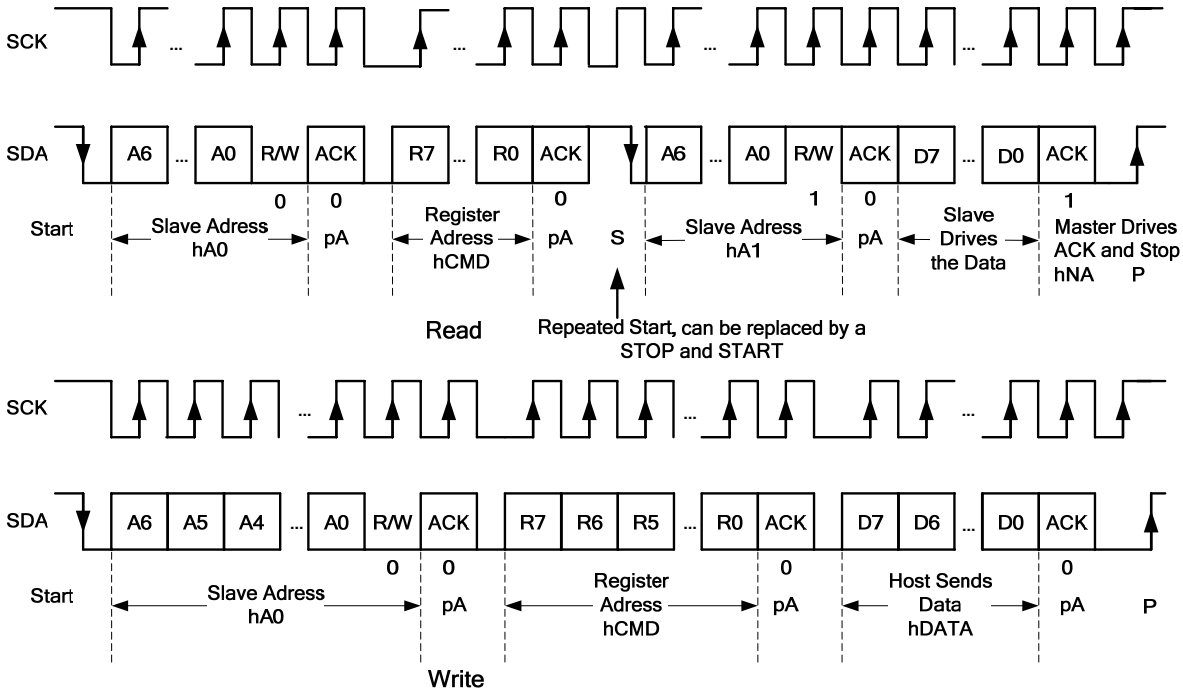
In the multi-cell applications,there maybe an external 5V converter,this pin can be set to the 5V converter

module enable signal(EN_EXT5V),when power on, the EN_EXT5V signal will set to high first,when 5V is stable,the AXP152's output will be enabled.When power off,after AXP152's output disabled 8ms later,EN_EXT5V goes to low.

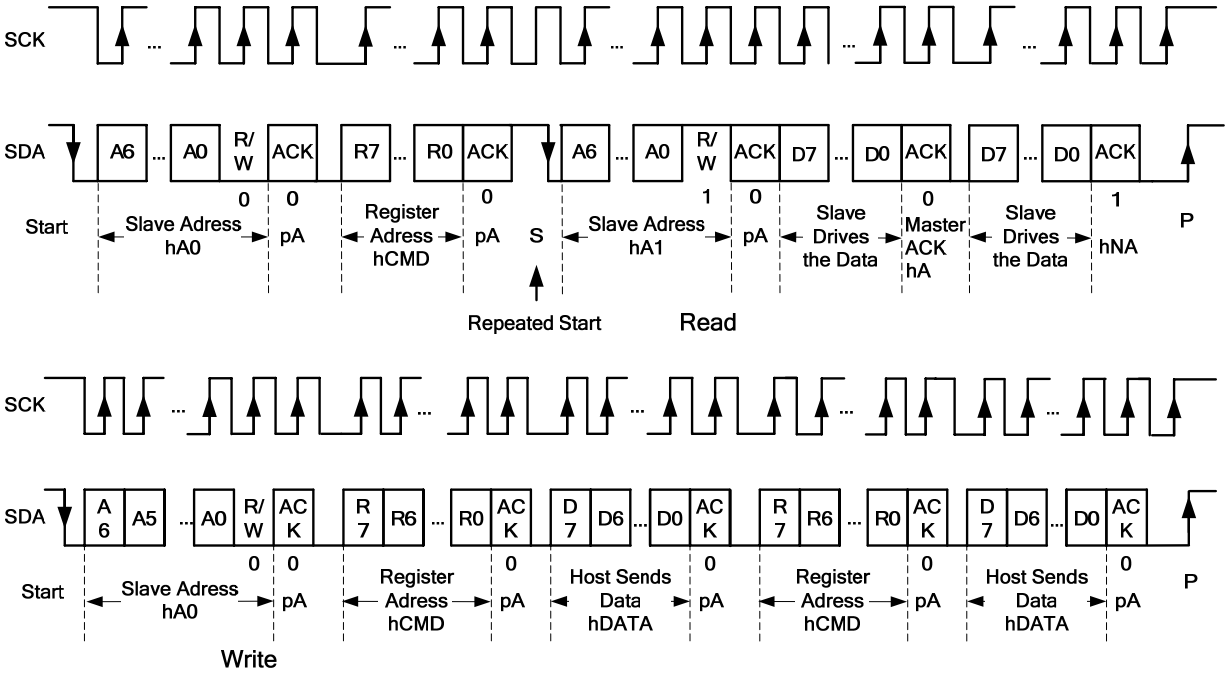
9.5 Timer

AXP152 features a 7-bit internal timer, whose values can be programmed via register REG8AH[6:0]. The minimum time step is one minute, and the timing range is 1~127 minutes.

9.6 TWSI and IRQ



PIC1:Single Read and Write



PIC2:Multi Read and Write

Host can visit AXP152 registers via the TWSI interface, and the operation timing is listed above. Standard 100KHz or 400KHz frequency is supported, and the highest rate can reach 1.2MHz. In addition, multi read and write operation is supported, and the device addresses are 61H (Read) and 60H (Write).

When certain events occur, AXP152 will inform Host by pulling down the IRQ interrupt mechanism, and the interrupt state will be reserved in interrupt state registers (See registers REG48H, REG49H, REG4AH). The interrupt can be cleared by writing 1 to corresponding state register bit. When there is no interrupt, IRQ output will be pulled high (51K resistance higher through the external). Each interrupt can be masked via interrupt control registers (Refer to registers REG40H, REG41H, REG42H,).

Item	IRQ No	Description
Reg48H[7]	Reserved,do not change	
Reg 48H[6]	IRQ1	LDO0IN insert IRQ
Reg 48H[5]	IRQ2	LDO0IN remove IRQ
Reg 48H[4]	Reserved,do not change	
Reg 48H[3]	IRQ3	ALDOIN insert IRQ
Reg 48H[2]	IRQ4	ALDOIN remove IRQ
Reg 48H[1]	Reserved,do not change	
Reg 48H[0]	Reserved,do not change	
Reg 49H[7]	Reserved,do not change	
Reg 49H[6]	Reserved,do not change	

Reg 49H[5]	IRQ5	DCDC1 voltage lower than 90% IRQ
Reg 49H[4]	IRQ6	DCDC2 voltage lower than 90% IRQ
Reg 49H[3]	IRQ7	DCDC3 voltage lower than 90% IRQ
Reg 49H[2]	IRQ8	DCDC4 voltage lower than 90% IRQ
Reg 49H[1]	IRQ9	Short-press key IRQ
Reg 49H[0]	IRQ10	Long-press key IRQ
Reg 4AH[7]	IRQ11	Timer timeout IRQ
Reg 4AH[6]	IRQ12	PEK positive edge IRQ
Reg 4AH[5]	IRQ13	PEK negative edge IRQ
Reg 4AH[4]	Reserved,do not change	
Reg 4AH[3]	IRQ14	GPIO3 edge IRQ
Reg 4AH[2]	IRQ15	GPIO2 edge IRQ
Reg 4AH[1]	IRQ16	GPIO1 edge IRQ
Reg 4AH[0]	IRQ17	GPIO0 edge IRQ

9.7 Registers

Type 1，Power Control Registers

Address	Description	R/W	Default
01	Power mode and Power on source indicate register	R	
12	DC-DC1/2/3/4 & ALDO1/2&DLDO1/2 control register	R/W	XX
13	ALDO1/2 work mode control register	R/W	00H
15	LDO0 control register	R/W	00H
23	DC-DC2 voltage set register	R/W	XX
25	DC-DC2 DVM parameter set register	R/W	00H
26	DC-DC1 voltage set register	R/W	XX
27	DC-DC3 voltage set register	R/W	XX
28	ALDO1/2 voltage set register	R/W	XX
29	DLDO1 voltage set register	R/W	XX
2A	DLDO2 voltage set register	R/W	XX
2B	DCDC4 voltage set register	R/W	XX
31	Wakeup and Voff set register	R/W	07H
32	Power off and sequence set register	R/W	00H
36	POK parameter set register	R/W	9DH
37	DCDC switch frequency set register	R/W	XX
80	DCDC switch mode set register	R/W	00H
81	Off-discharge and output monitor set register	R/W	FDH
8A	Timer control register	R/W	00H
8F	IRQ wakeup and over-temperature off set register	R/W	01H

Type 2，GPIO Control Registers

Address	Description	R/W	Default
90	GPIO0 set register	R/W	07H
91	GPIO1 set register	R/W	07H
92	GPIO2 set register	R/W	07H
93	GPIO3 set register	R/W	07H
96	GPIO2 LDO mode output voltage set register	R/W	0AH
97	GPIO[3:0] input status register	R/W	00H
98	PWM0 frequency set register	R/W	00H
99	PWM0 duty set register 1	R/W	16H
9A	PWM0 duty set register 2	R/W	0BH
9B	PWM1 frequency set register	R/W	00H
9C	PWM1 duty set register 1	R/W	16H
9D	PWM1 duty set register 2	R/W	0BH

Type 3，IRQ Control Registers

Address	Description	R/W	Default
40	IRQ enable set register 1	R/W	00H
41	IRQ enable set register 2	R/W	03H
42	IRQ enable set register 3	R/W	00H
48	IRQ status register 1	R/W	00H
49	IRQ status register 2	R/W	00H
4A	IRQ status register 3	R/W	00H

REG 01H: Power mode and Power on source indicate register

Bit	Descrption	R/W
7-6	Reserved,do not change	R
5	When LDO0EN=high,LDO0IN status 0:LDO0IN not present(<3.5V)； 1:LDO0IN present(>3.8V)	R
4	SIEN 0:can’t use TWSI 1:use TWSI	R
3	IRQ pin triggled power on	R
2	PWRON key triggled power on	R
1	Reserved,do not change	R

0	ALDOIN 上升沿触发开机指示	R

REG 12H:Output control register

Bit	Description		R/W	Default
7	DC-DC1 Enable	0:disable 1:Enable	RW	XX
6	DC-DC2 Enable		RW	
5	DC-DC3 Enable		RW	
4	DC-DC4 Enable		RW	
3	ALDO1 Enable		RW	
2	ALDO2 Enable		RW	
1	DLDO1 Enable		RW	
0	DLDO2 Enable		RW	

REG 13H: ALDO1/2 work mode control register

Bit	Description		R/W	Default
7-4	Reserved,do not change			
3	ALDO1 work mode	0:low noise mode 1:low power mode	RW	0
2	ALDO2 work mode		RW	0
1-0	Reserved,do not change		RW	00

REG 15H:LDO0 control register

Bit	Description		R/W	Default
7	LDO0 enable	0:disable 1:enable When LDO0EN=LDO0IN,this bit will be ignored	RW	0
6	Reserved,do not change		RW	0
5	LDO0 voltage set bit1	00:5V; 01:3.3V; 10:2.8V; 11:2.5V	RW	0
4	LDO0 voltage set bit0		RW	0
3-2	Reserved,do not change		RW	0
1	LDO0 current limited set bit1	00:do not limit 01:1500mA 10:900mA 11:500mA	RW	0
0	LDO0 current limited set bit0		RW	0

REG 23H:DC-DC2 output voltage set register

Bit	Description		R/W	Default
7-6	Reserved,do not change		RW	0
5~0	DC-DC2 output voltage set bit5~0	0.7-2.275V，25mV/step	RW	XX

REG 25H:DC-DC2 DVM parameter set register

Bit	Description		R/W	Default
7-3	Reserved,do not change			
2	DC-DC2 DVM enable	0:disable 1:enable	RW	0
1	Reserved,do not change		RW	0
0	DC-DC2 DVM ramp control	0: 25mV/15.625us=1.6mV/us 1: 25mV/31.250us=0.8mV/us	RW	0

REG 26H:DC-DC1 output voltage set register

Bit	Description		R/W	Default
7-4	Reserved,do not change			
3	DC-DC1 output voltage set bit3	0000:1.7V;0001:1.8V;0010:1.9V;0011:2.0V; 0100:2.1V;0101:2.4V;0110:2.5V;0111:2.6V; 1000:2.7V;1001:2.8V;1010:3.0V;1011:3.1V; 1100:3.2V;1101:3.3V;1110:3.4V;1111:3.5V;	RW	XX
2	DC-DC1 output voltage set bit2		RW	
1	DC-DC1 output voltage set bit1		RW	
0	DC-DC1 output voltage set bit0		RW	

REG 27H:DC-DC3 output voltage set register

Bit	Description		R/W	Default
7-6	Reserved,do not change		RW	0
5	DC-DC3 output voltage set bit5~0	0.7-3.5V，50mV/step	RW	XX& DC3SET

REG 28H:ALDO1/2 output voltage set register

Bit	Description		R/W	Default
7	ALDO1 output voltage set bit3	0000:1.2V;0001:1.3V;0010:1.4V;0011:1.5V; 0100:1.6V;0101:1.7V;0110:1.8V;0111:1.9V; 1000:2.0V;1001:2.5V;1010:2.7V;1011:2.8V;	RW	XX
6	ALDO1 output voltage set bit2		RW	
5	ALDO1 output voltage set bit1		RW	

4	ALDO1 output voltage set bit0	1100:3.0V;1101:3.1V;1110:3.2V;1111:3.3V;	RW	
3	ALDO2 output voltage set bit3	0000:1.2V;0001:1.3V;0010:1.4V;0011:1.5V;	RW	
2	ALDO2 output voltage set bit2	0100:1.6V;0101:1.7V;0110:1.8V;0111:1.9V;	RW	
1	ALDO2 output voltage set bit1	1000:2.0V;1001:2.5V;1010:2.7V;1011:2.8V;	RW	
0	ALDO2 output voltage set bit0	1100:3.0V;1101:3.1V;1110:3.2V;1111:3.3V;	RW	

REG 29H:DLDO1 output voltage set register

Bit	Description		R/W	Default
7	DLDO1 mode control	0:LDO mode，refer to bit[4:0] 1:Switch mode，VIN is DLDOIN	RW	0
6~5	Reserved,do not change		RW	0
4~0	DLDO1 output voltage set bit4~0	0.7~3.5V,100mV/step	RW	XX

REG 2AH:DLDO2 output voltage set register

Bit	Description		R/W	Default
7	DLDO2 mode control	0:LDO mode,refer to bit[4:0] 1:Switch mode,VIN is DLDOIN	RW	0
6~5	Reserved,do not change		RW	0
4~0	DLDO2 output voltage set bit4~0	0.7~3.5V,100mV/step	RW	XX

REG 2BH:DCDC4 output voltage set register

Bit	Description		R/W	Default
7	Reserved,do not change		RW	0
6~0	DCDC4 output voltage set bit6~0	0.7~3.5V,25mV/step	RW	XX

REG 31H: Power recovery and V_{OFF} voltage set register

Bit	Description		R/W	Default
7	PWROK go low or not when power recovery	0:PWROK do not go low 1:go low when wakeup	RW	0
6~4	Reserved,do not change		RW	000

3	Power recovery enable	0:disable 1:enable	RW	0
2	V_{OFF} voltage set bit2	000:2.6V;001:2.7V;010:2.8V;011:2.9V 100:3.0V;101:3.1V;110:3.2V;111:3.3V	RW	111
1	V_{OFF} voltage set bit1			
0	V_{OFF} voltage set bit0			

REG 32H: Power off and sequence set register

Bit	Description		R/W	Default
7	Power off	Write 1 to this bit will power off the AXP152	RW	0
6~3	Reserved,do not change		RW	0000
2	Power off sequence	0:all outputs power off the sametime 1:reverse sequence of the power on	RW	0
1~0	Reserved,do not change		RW	00

REG 36H: PEK parameter set register

Bit	Description		R/W	Default
7~6	ONLEVEL set bit1~0	00:128ms; 01:3s; 10:1s; 11:2s;	RW	10
5~4	IRQLEVEL set bit1~0	00:1s; 01:1.5s; 10:2s; 11:2.5s;	RW	01
3	PEK>OFFLEVEL,power off function set	0:disable 1:enable	RW	1
2	PWROK delay after all outputs stable	0:8ms 1:64ms	RW	1
1~0	OFFLEVEL set	00:4s; 01:6s; 10:8s; 11:10s	RW	01

REG 37H: DCDC switch frequency set register

Bit	Description		R/W	Default
7	DCDC frequeny spread enable	0:disable 1:enable	RW	XX
6	DCDC frequeny spread range control	0:50KHz 1:100KHz	RW	XX
5~4	Reserved,do not change		RW	00
3~0	DCDC frequency set bit3~0	Step:5%	RW	1000

REG 80H: DCDC work mode set register

Bit	Description		R/W	Default
7~4	Reserved,do not change		RW	0000
3	DCDC1 PFM/PWM mode control	0:auto switch mode 1:fixed PWM mode	RW	0
2	DCDC2 PFM/PWM mode control		RW	0
1	DCDC3 PFM/PWM mode control		RW	0
0	DCDC4 PFM/PWM mode control		RW	0

REG 81H: Off-discharge and output monitor set register

Bit	Description		R/W	Default
7	DCDC/LDO off discharge enable	0:disable 1:enable	RW	1
6	Reserved,do not change		RW	1
5	DCDC1 under 85% power off	0:disable 1:enable	RW	1
4	DCDC2 under 85% power off		RW	
3	DCDC3 under 85% power off		RW	
2	DCDC4 under 85% power off		RW	
1~0	DCDC1/2/3/4 output monitor debounce time set	00:62us;01:124us;10:186us;11:248us	RW	01

REG 8AH: Timer control register

Bit	Description		R/W	Default
7	Timer time out flag	1:timeout Write 1 to this bit will clear it	RW	0
6~0	Timer set	0~2^7 1 minute / step,timer off when value=0	RW	0000000

REG 8FH: IRQ PIN wakeup and over temperature power off set

Bit	Description		R/W	Default
7	IRQ Pin wakeup enable	0:disable 1:enable	RW	0
6~3	Reserved,do not change		RW	0000
2	Over temperature enable	0:disable 1:enable	RW	0

1~0	Over temperature power off threshold	00:106℃ 01:118℃ 10:130℃ 11:144℃	RW	01

REG 90H: GPIO0 control register

Bit	Description		R/W	Default
7	GPIO0 as digital input posedge triggle IRQ and wakeup enable	0:disable 1:enable	RW	0
6	GPIO0 as digital input negative edge IRQ and wakeup enable	0:disable 1:enable	RW	0
5~3	Reserved,do not change		RW	000
2~0	GPIO0 control bit2~0	000:Pull low 001:Pull high(high level same as DCDC1) 010:PWM0(high level same as DCDC1) 011:Digital input 100~111:Floating	RW	111

REG 91H: GPIO1 control register

Bit	Description		R/W	Default
7	GPIO1 as digital input posedge triggle IRQ and wakeup enable	0:disable 1:enable	RW	0
6	GPIO1 as digital input negative edge IRQ and wakeup enable	0:disable 1:enable	RW	0
5~3	Reserved,do not change		RW	000
2~0	GPIO1control bit2~0	000:Pull low 001:Pull high(high level same as DCDC1) 010:PWM0(high level same as DCDC1) 011:Digital input 100~111:Floating	RW	111

REG 92H: GPIO2 control register

Bit	Description		R/W	Default
7	GPIO2 as digital input posedge triggle IRQ and wakeup enable	0:disable 1:enable	RW	0
6	GPIO2 as digital input negative edge IRQ and wakeup enable	0:disable 1:enable	RW	0
5~3	Reserved,do not change		RW	000
2~0	GPIO2 control bit2~0	000:Pull low	RW	111

		001:Pull high(need external pull-up resistor) 010:Low noise LDO 011:Digital input 100~111:Floating		

REG 93H: GPIO3(PWREN) control register

Bit	Description		R/W	Default
7	GPIO3 as digital input posedge triggle IRQ and wakeup enable	0:disable 1:enable	RW	0
6	GPIO3 as digital input negative edge IRQ and wakeup enable	0:disable 1:enable	RW	0
5~4	Reserved,do not change		RW	00
3	GPIO3 Pin function select	0:PWREN function 1:GPIO3	RW	0
2~0	GPIO3 control bit2~0	000:Pull low 001:Pull high(need external pull-up resistor) 010:Floating 011:Digital input 100~111:Floating	RW	111

REG 96H: GPIO2 LDO mode output voltage set register

Bit	Description		R/W	Default
7~4	Reserved,do not change			
3~0	GPIOLDO output voltage set bit3~0	0000:1.8V;0001:1.9V;0010:2.0V;0011:2.1V; 0100:2.2V;0101:2.3V;0110:2.4V;0111:2.5V; 1000:2.6V;1001:2.7V;1010:2.8V;1011:2.9V; 1100:3.0V;1101:3.1V;1110:3.2V;1111:3.3V;	RW	1010

REG 97H: GPIO[3:0] input status

Bit	Description		R/W	Default
7~4	Reserved,do not change			
3	GPIO3 input status		R	0
2	GPIO2 input status		R	0
1	GPIO1 input status		R	0
0	GPIO0 input status		R	0

REG 98H: PWM0 frequency set register

Bit	Description		R/W	Default
7~0	PWM0 output frequency set(X0)	0~255	RW	00H

REG 99H: PWM0 duty denominator set register

Bit	Description		R/W	Default
7~0	PWM0 duty denominator set(Y0)	1~255	RW	16H

REG 9AH: PWM0 duty numerator set register

Bit	Description		R/W	Default
7~0	PWM0 duty numerator set(Z0)	0~Y0	RW	0BH

注：PWM0 frequency = 2.25MHz/(X0+1)/Y0
PWM0 duty = Z0/Y0

REG 9BH: PWM1 frequency set register

Bit	Description		R/W	Default
7~0	PWM1 output frequency set(X1)	0~255	RW	00H

REG 9CH: PWM1 duty denominator set register

Bit	Description		R/W	Default
7~0	PWM1 duty denominator set(Y1)	1~255	RW	16H

REG 9DH: PWM1 duty numerator set register

Bit	Description		R/W	Default

7~0	PWM1 duty numerator set(Z1)	0~Y0	RW	0BH

注：PWM1 frequency = 2.25MHz/(X1+1)/Y1
PWM1 duty = Z1/Y1

REG 40H: IRQ enable 1

Bit	Description	R/W	Default
7	Reserved,do not change	RW	0
6	LDO0IN insert IRQ enable(LDO0EN connect to LDO0IN)	RW	0
5	LDO0IN remove IRQ enable(LDO0EN connect to LDO0IN)	RW	0
4	Reserved,do not change	RW	0
3	ALDOIN insert IRQ enable	RW	0
2	ALDOIN remove IRQ enable	RW	0
1-0	Reserved,do not change	RW	0

REG 41H: IRQ enable 2

Bit	Description	R/W	Default
7-6	Reserved,do not change	RW	0
5	DCDC1 voltage lower than 90% IRQ enable	RW	0
4	DCDC2 voltage lower than 90% IRQ enable	RW	0
3	DCDC3 voltage lower than 90% IRQ enable	RW	0
2	DCDC4 voltage lower than 90% IRQ enable	RW	0
1	Short-press key IRQ enable	RW	1
0	Long-press key IRQ enable	RW	1

REG 42H: IRQ enable 3

Bit	Description	R/W	Default
7	Timer timeout IRQ enable	RW	0
6	PWRON key posedgeIRQ enable	RW	0
5	PWRON key negedge IRQ enable	RW	0
4	Reserved,do not change	RW	0
3	GPIO3 input edge IRQ enable	RW	0
2	GPIO2 input edge IRQ enable	RW	0
1	GPIO1 input edge IRQ enable	RW	0
0	GPIO0 input edge IRQ enable	RW	0

REG 48H: IRQ status 1

Bit	Description	R/W	Default
7	Reserved,do not change	RW	0
6	LDO0IN insert IRQ	RW	0
5	LDO0IN remove IRQ	RW	0
4	Reserved,do not change	RW	0
3	ALDOIN insert IRQ	RW	0
2	ALDOIN remove IRQ	RW	0
1-0	Reserved,do not change	RW	0

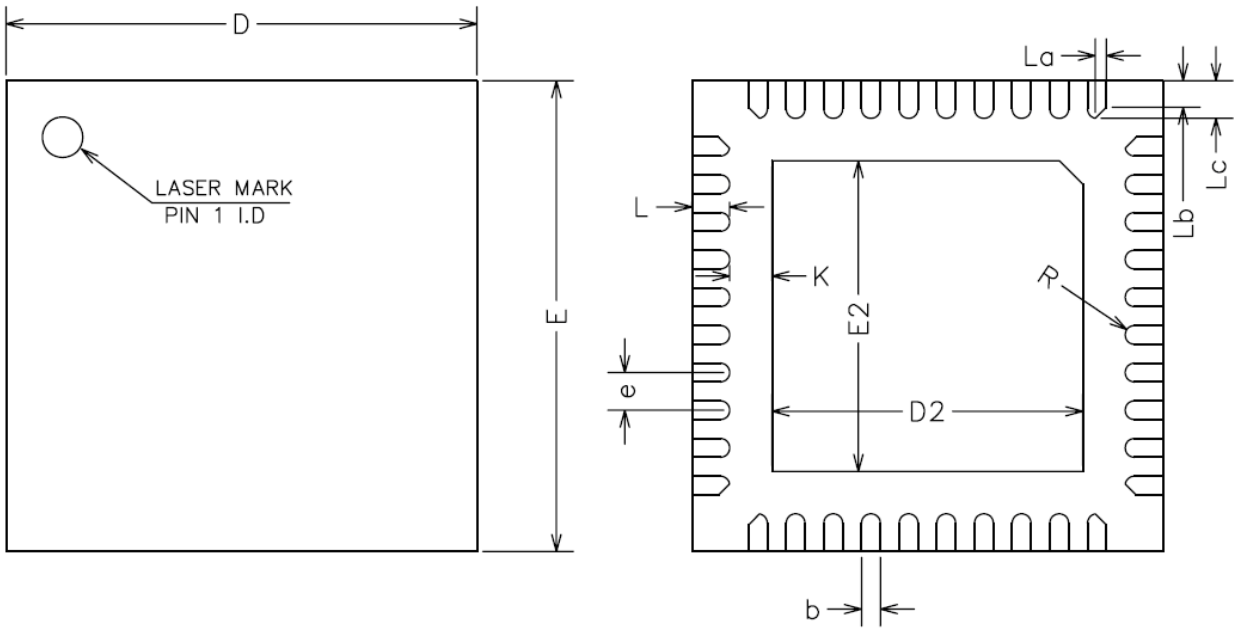
REG 49H: IRQ status 2

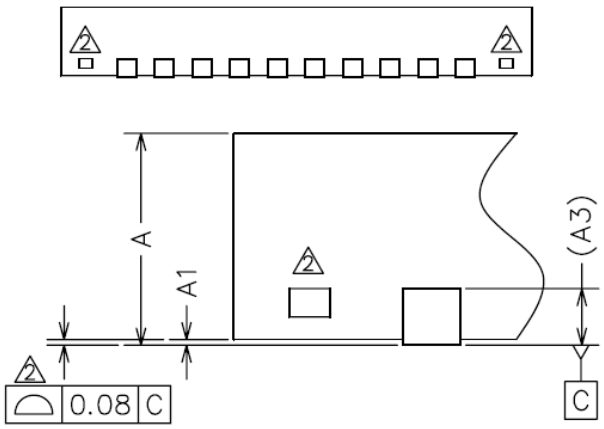
Bit	Description	R/W	Default
7-6	Reserved,do not change	RW	0
5	DCDC1 voltage lower than 90% IRQ	RW	0
4	DCDC2 voltage lower than 90% IRQ	RW	0
3	DCDC3 voltage lower than 90% IRQ	RW	0
2	DCDC4 voltage lower than 90% IRQ	RW	0
1	Short-press key IRQ	RW	0
0	Long-press key IRQ	RW	0

REG 4AH: IRQ status 3

Bit	Description	R/W	Default
7	Timer timeout IRQ	RW	0
6	PWRON key posedge IRQ	RW	0
5	PWRON key negedge IRQ	RW	0
4	Reserved,do not change	RW	0
3	GPIO3 input edge IRQ	RW	0
2	GPIO2 input edge IRQ	RW	0
1	GPIO1 input edge IRQ	RW	0
0	GPIO0 input edge IRQ	RW	0

10 . Package





SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20REF	
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.15	3.30	3.45
E2	3.15	3.30	3.45
e	0.30	0.40	0.50
K	0.20	–	–
L	0.30	0.40	0.50
R	0.09	–	–
La	0.12	0.15	0.18
Lb	0.23	0.26	0.29
Lc	0.30	0.39	0.50